WE CLAIM:

1. An integrated circuit (IC) chip, comprising:

a useful circuit having a component that is subject to failure in response to operational stress; and

a prognostic cell that is statistically designed to fail under increased operational stress correlated to the operational stress on the useful circuit by a prognostic distance ahead of the useful circuit, said cell triggering a failure indicator as a predictor of impending failure of the useful circuit.

2. The IC chip of claim 1, wherein the prognostic cell comprises:

a test device having a test component;

a coupling circuit that couples the operational stress applied to the useful circuit to the test device;

a stress circuit that increases the operational stress applied to the test device to accelerate deterioration of the test component; and

a comparison circuit that compares a performance characteristic of the stressed test component to the baseline, determines whether the stressed test component has failed and generates the failure indicator.

3. The IC chip of claim 2, wherein the useful circuit and the test device are equivalent devices.

4. The IC chip of claim 2, wherein the useful circuit and the test device are different devices with similar components.

5. The IC chip of claim 4, wherein the useful circuit's

component is a gate insulator of a transistor and the test component is a spacer insulator layer of a capacitor.

6. The IC chip of claim 4, wherein the test component has different dimensions than the useful circuit's component to enhance measurement sensitivity.

7. The IC chip of claim 2, wherein the coupling circuit couples the test device to at least one of a supply voltage, a drive signal or a stress event outside normal operating condition applied to the useful circuit.

8. The IC chip of claim 7, wherein the stress circuit increases said supply voltage, alters said drive signal or prolongs the stress event to increase the operational stress applied to the test device.

9. The IC chip of claim 2, wherein the prognostic cell comprises a plurality of test devices, said comparison circuit triggering the failure indicator when a certain fraction of the plurality fail.

10. The IC chip of claim 9, wherein said comparison circuit reads out each test device failure.

11. The IC chip of claim 2, further comprising a reference circuit that is subjected to reduced operation stress to establish the baseline for the performance characteristic.

12. The IC chip of claim 11, wherein the reference sub-circuit is subjected to minimal operational stress.

13. The IC chip of claim 12, wherein the reference sub-circuit is subjected to average operational stress.

14. The IC chip of claim 1, wherein the increased operational stress accelerates an end-of-life failure mechanism of the prognostic cell.

15. The IC chip of claim 1, wherein the prognostic distance is a design parameter and the increased operational stress is a function of that design parameter.

16. The IC chip of claim 15, wherein the increased operational stress applied to the prognostic cell is the same operational stress that is applied to the useful circuit just increased so that the failure of the prognostic cell, although accelerated, tracks the failure of the useful circuit.

17. The IC chip of claim 15, wherein the operational stress comprises use stress and environmental stress.

18. The IC chip of claim 17, wherein the operational stress is increased by an elevated supply voltage, a different bias condition or a modified drive signal applied to the test device.

19. The IC chip of claim 1, wherein the useful circuit's component has a cumulative failure probability C(t) and the prognostic cell has a cumulative trigger probability P(t), t1 equals the time at which a fraction f1 of the prognostic cells have triggered, t2 equals the time at which the failure probability of the useful circuit's component has increased to a fraction f2, said prognostic distance being equal to t2-t1.

20. The IC chip of claim 19, wherein f1 is the tolerable fraction of non-accurate predictions by the prognostic cell and f2 is the tolerable failure fraction of the useful circuit's component.

21. The IC chip of claim 20, wherein the prognostic cell is stressed so that P(t) reaches a value close to unity before C(t) start to increase appreciably.

22. The IC chip of claim 19, wherein the prognostic cell has a trigger probability density p(t) with a standard deviation that affects an amount of useful lifetime sacrificed by a premature trigger and/or a fraction of missed failure predictions of the useful circuit's component by late triggers.

23. The IC chip of claim 22, wherein the fraction f1 is set close to unity so that the fraction of missed failure predictions is small.

24. The IC chip of claim 22, wherein the trigger probability density p(t) overlaps with a failure probability density c(t) of the useful circuit's component, said fraction f1 being set so that the prognostic distance is positive and small.

25. The IC chip of claim 22, wherein the prognostic cell comprises a plurality of test devices with test components that fail the same performance characteristic, said cell triggering the failure indicator when a certain fraction of the plurality fail thereby reducing the standard deviation of p(t) and the amount of useful lifetime sacrificed.

26. The IC chip of claim 19, wherein the prognostic cell has a trigger probability density p(t) with a standard deviation that affects the accuracy of triggering the failure indicator, said prognostic cell comprising a plurality of test devices with test components that fail the same performance characteristic, said cell triggering the failure indicator when a certain fraction of the plurality fail thereby reducing the standard deviation of p(t) and improving the accuracy of the failure indicator.

27. The IC chip of claim 1, wherein the prognostic cell predicts failure of a gate insulator in a MOS device based on an ESD event, said prognostic cell comprising a test capacitor having an insulator spacer layer, a coupling circuit that couples a supply voltage and the ESD event to the test capacitor, a stress circuit that increases the supply voltage to the test capacitor and prolongs the ESD event, and a comparison sub-circuit that compares the voltage supported across the test capacitor against a baseline voltage to detect degradation of the insulator spacer layer.

28. The IC chip of claim 27, wherein the coupling circuit comprises at least one diode that is forward biased by an ESD event to couple it to the test capacitor and the stress circuit comprises a charge pump that increases the supply voltage and sufficient capacitance to prolong the ESD event across the test capacitor.

29. The IC chip of claim 28, wherein the charge pump is periodically disconnected to allow the voltage across the test capacitor to degrade, said comparison circuit comparing this

voltage against the baseline voltage to detect degradation of the insulator spacer layer.

30. The IC chip of claim 1, wherein the prognostic cell predicts leakage under the field oxide failure of a MOS device in the host IC based on radiation effects, said prognostic cell comprising at least one of:

a first inverter formed by a current source and a monitor transistor having a gate bias to stress the radiated transistor, said current source being set to an allowed radiation degradation limit for end around leakage between the monitor transistor's source and drain;

a second inverter formed by a current source and a monitor transistor having a gate bias to stress the radiated transistor, said current source being set to an allowed radiation degradation limit for device to device leakage in a common well;

a third inverter formed by a current source and a monitor transistor having a gate bias to stress the radiated transistor, said current source being set to an allowed radiation degradation limit for device to a neighboring n-well leakage; and

a comparator generating the failure indicator when any one of the inverters produces an output that inverts with respect to the baseline.

31. The IC chip of claim 1, wherein the prognostic cell predicts threshold voltage shift of a MOS device in the host IC based on radiation effects, said prognostic cell comprising test and reference MOS devices with different gate bias conditions so that the MOS devices exhibit different threshold voltage shifts when subjected to ionizing radiation, and a

comparator circuit that generates the failure indicator when the difference in threshold voltages exceeds a preset amount.

32. The IC chip of claim 31, wherein a worst case gate bias is applied to the test MOS device and a best case gate bias is applied to the reference MOS device.

33. The IC chip of claim 1, wherein the prognostic cell predicts time dependent dielectric breakdown (TDDB) of an insulator layer in the host IC based on the insulator electric field, said prognostic cell comprising a test capacitor with an insulator spacer layer, a coupling circuit that couples a supply voltage from the host IC to the test capacitor, a stress circuit that increases the supply voltage applied to the test capacitor to create a stressed insulator electric field, and a comparison circuit that compares the voltage supported across the test capacitor against a baseline voltage to detect degradation of the insulator spacer layer.

34. The IC chip of claim 33, wherein the stress circuit comprises a charge pump that pumps a well containing the test capacitor to create a larger voltage across the insulator spacer layer than the supply voltage.

35. The IC chip of claim 34, wherein the charge pump is periodically disconnected to allow the voltage across the test capacitor to degrade, said comparison circuit comparing this voltage against the baseline voltage to detect degradation of the insulator spacer layer.

36. The IC chip of claim 1, wherein the prognostic cell predicts hot carrier degradation of MOS transistors in the

host IC, said prognostic cell comprising test and reference MOS devices with different gate voltages so that the MOS transistors exhibit, over time, different threshold voltage shifts, and a comparator circuit that generates the failure indicator when the difference in threshold voltages exceeds a preset amount.

37. The IC chip of claim 36, wherein the gate voltage of the test MOS device is approximately one third of the drain voltage for longer periods than the gate voltage of the reference MOS device.

38. The IC chip of claim 37, wherein the gate voltage of the test MOS device is a triangular wave.

39. The IC chip of claim 1, wherein the prognostic cell predicts metal migration of interconnect conductors in the host IC.

40. An integrated circuit (IC) chip, comprising:

a useful circuit having a component that is subject to failure in response to operational stress; and

a prognostic cell that is statistically designed to fail under increased operational stress by a prognostic distance ahead of the useful circuit component, said prognostic cell comprises:

a plurality of test devices each having a test component;

a coupling circuit that couples the operational stress applied to the useful circuit to the test devices;

a stress circuit that increases the operational stress applied to the test devices as a function of the

prognostic distance to accelerate deterioration of the test components; and

a comparison circuit that compares a performance characteristic of each test component to a baseline, determines whether the stressed test component has failed and when a certain fraction of the plurality fail generates a failure indicator as a predictor of impending failure of the useful circuit.

41. The IC chip of claim 40, wherein the coupling circuit couples the test device to at least one of a supply voltage, a drive signal or a stress event outside normal operating condition applied to the host device, and the stress circuit increases said supply voltage, alters said drive signal or prolongs the stress event to increase the operational stress applied to the test device.

42. The IC chip of claim 40, wherein said comparison circuit reads out each test device failure.

43. The IC chip of claim 40, further comprising a reference circuit that is subjected to reduced operational stress to establish the baseline for the performance characteristic.

44. The IC chip of claim 40, wherein the test component has a trigger probability density p(t) with a standard deviation that affects an amount of useful lifetime sacrificed by a premature trigger, the number of test devices being such that the amount of useful lifetime sacrificed is less than an acceptable amount.

45. An integrated circuit (IC) chip, comprising:

a useful circuit having a component that is subject to failure in response to operational stress; and

an oversampled prognostic cell with multiple readout capability that is statistically designed to fail under increased operational stress by a prognostic distance ahead of the useful circuit component, said prognostic cell comprises:

a plurality of test devices each having a test component;

a coupling circuit that couples the operational stress applied to the useful circuit to the test devices;

a stress circuit that increases the operational stress applied to the test devices as a function of the prognostic distance to accelerate deterioration of the test components; and

a comparison circuit that compares a performance characteristic of each test component to a baseline, determines whether the stressed test component has failed and generates a failure indicator for each failed test component.

46. The IC chip of claim 45, further comprising a reference circuit that is subjected to reduced operational stress to establish the baseline for the performance characteristic.

47. The IC chip of claim 45, wherein the test component has a trigger probability density p(t) with a standard deviation that affects an amount of useful lifetime sacrificed by a premature trigger, the number of test devices being such that the amount of useful lifetime sacrificed is less than an acceptable amount.

48. A integrated circuit (IC) chip comprising:

At least one MOS transistor having a gate insulator layer

that is subject to failure in response to operational stress in part related to a supply voltage Vdd;

an input pin for communicating a voltage signal to the useful circuit;

an ESD clamp for dampening spikes in the voltage signal caused by ESD events, any insufficiently dampened spikes further stressing the useful circuit;

an ESD prognostic cell comprising;

a node;

a test capacitor having a spacer insulator layer;

a voltage circuit that increases the supply voltage Vdd to a stress voltage Vs at the node to place an amount of excess stress on the test capacitor's spacer insulator layer;

a diode between the input pin and node that couples the spike in the voltage signal caused by the ESD event to the node thereby further raising the stress voltage Vs; and

a comparator that compares the voltage supported by the test capacitor against a baseline and triggers a failure indicator when the difference exceeds a threshold.

49. The IC chip of claim 48, wherein the voltage circuit comprises a charge pump.

50. The IC chip of claim 48, wherein the test capacitor breaks down and is unable to support the stress voltage.

51. The IC chip of claim 48, wherein the voltage circuit is periodically disconnected to allow the voltage across the test capacitor to degrade, said comparison circuit comparing this voltage against the baseline voltage to detect degradation of the insulator spacer layer.

52. A integrated circuit (IC) chip comprising:

At least one useful circuit having an insulator layer that is subject to failure in response to operational stress in part related to a supply voltage Vdd;

A time dependent dielectric breakdown (TDDB) prognostic cell comprising;

a node;

a test capacitor having a spacer insulator layer;

a voltage circuit that increases the supply voltage Vdd to a stress voltage Vs at the node to place an amount of excess stress on the test capacitor's spacer insulator layer; and

a comparator that compares the voltage supported by the test capacitor against a baseline and triggers a failure indicator when the difference exceeds a threshold.

53. The IC chip of claim 52, wherein the voltage circuit comprises a charge pump.

54. The IC chip of claim 52, wherein the test capacitor breaks down and is unable to support the stress voltage.

55. The IC chip of claim 52, wherein the voltage circuit is periodically disconnected to allow the voltage across the test capacitor to degrade, said comparison circuit comparing this voltage against the baseline voltage to detect degradation of the insulator spacer layer.

56. The IC chip of claim 52, further comprising a feedback loop from the comparator to the voltage circuit to disable the voltage circuit upon triggering of the failure indicator.

57. An integrated circuit (IC) chip, comprising:

a MOS transistor having a field oxide that degrades due to radiation effects;

a field leakage radiation prognostic cell comprising at least one of:

a first inverter formed by a current source and a monitor transistor having a gate bias selected to apply excess stress to the monitor transistor, said current source being set to an allowed radiation degradation limit for end around leakage between the monitor transistor's source and drain;

a second inverter formed by a current source and a monitor transistor having a gate bias selected to apply excess stress to the monitor transistor, said current source being set to an allowed radiation degradation limit for device to device leakage in a common well;

a third inverter formed by a current source and a monitor transistor having a gate bias selected to apply excess stress to the monitor transistor, said current source being set to an allowed radiation degradation limit for device to a neighboring n-well leakage; and

a comparator that generates a failure indicator when any one of the inverters produces an output that inverts with respect to a baseline.

58. The IC chip of claim 57, wherein for each inverter if the monitor transistor has not degraded the current from the current source will keep the drain voltage high but if the monitor transistor has degraded the transistor will sink the current and the drain voltage will invert low.

59. The IC chip of claim 57, wherein the prognostic cell comprises all three inverters.